MOTOROLA
Semiconductor Products Inc.

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Application Note

SYNCHRONOUS I/O FOR THE MC68000 USING THE MC6852

Prepared by:
James McKenzie
Microprocessor Applications Engineering
Austin, Texas

The MC6852 Synchronous Serial Data Adapter (SSDA) provides both a synchronous serial transmitter and synchronous serial receiver in a single, 24-pin device. Synchronous data communications is inherently more efficient than asynchronous data communications because each character need not be framed for error detection. Hence, synchronous data communications lends itself to higher data rates and applications which are synchronous in nature, such as serial communications between synchronous processors.

The SSDA is particularly well-suited for data communications applications involving byte-oriented protocols such as Bisync. Both the SSDA transmitter and receiver are interfaced to a single 8-bit bidirectional data bus. Data to be transmitted is loaded from the MPU data bus into a 3-byte FIFO on the SSDA. An 8-bit shift register is used to serially transmit data from the last FIFO location; parity may also be appended. Received data enters another 8-bit shift register where parity may be checked. Data from the shift register enters a 3-byte receiver FIFO which presents the data in parallel form to the MPU bus.

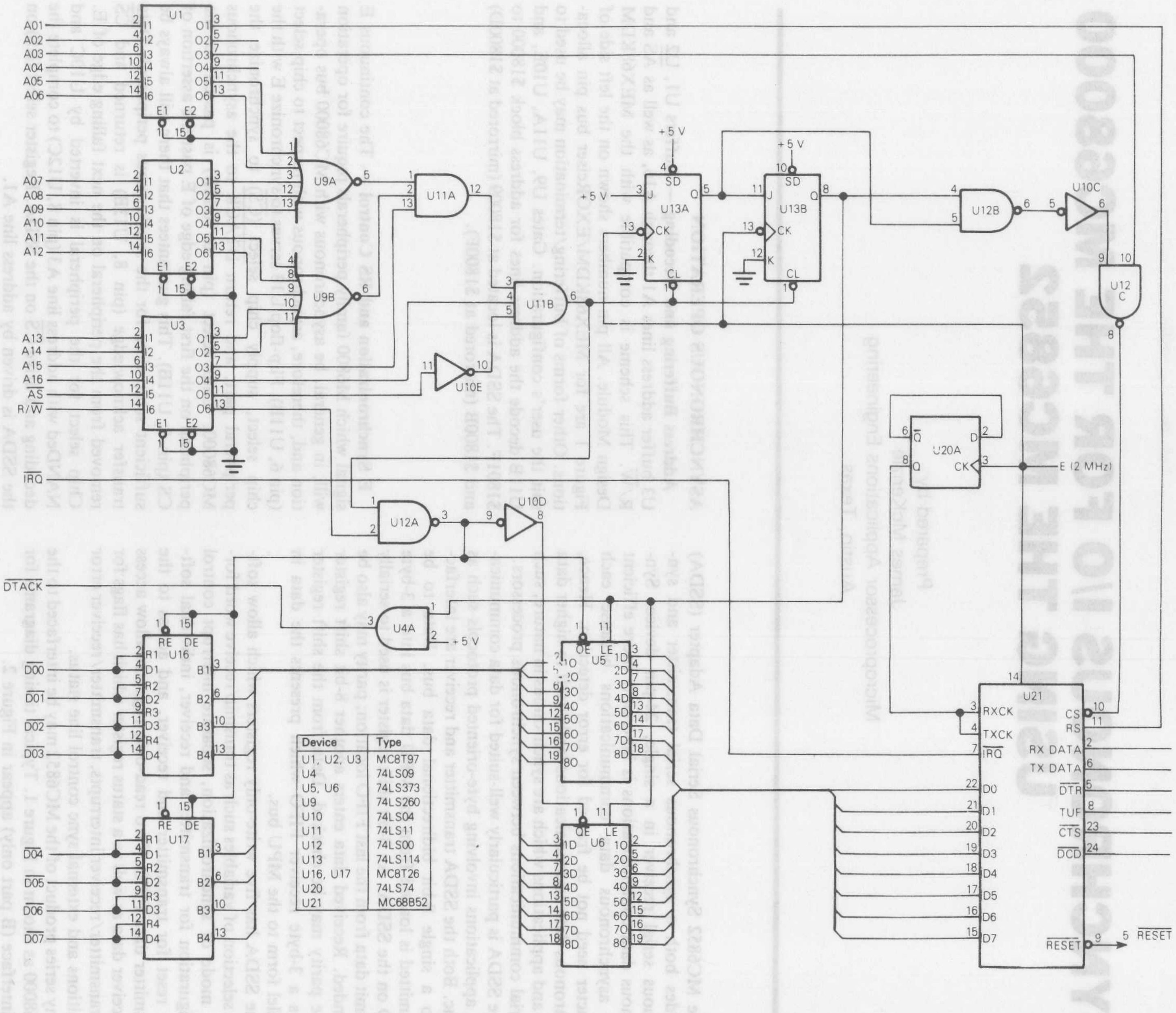
The SSDA has five write-only registers which allow software selection of variables such as transmit/receive word format, mode of synchronization, separate interrupt control configuration for transmitter and receiver, individual software reset for transmitter and receiver, and access to the transmitter data FIFO. Two read-only registers allow access to receiver data as well as a status register which has flags for the transmitter/receiver interrupts, transmitter/receiver error conditions and external sync control line status.

Any series product of the MC6852 may be interfaced to the MC68000 as shown in Figure 1. Typical timing diagrams for this interface (B part only) appear in Figure 2.

ASYNCHRONOUS OPERATION

Address Buffering and Decoding — Buffers U1, U2 and U3 buffer address lines A1 through A16, as well as $\overline{\text{AS}}$ and R/$\overline{\text{W}}$. This scheme is compatible with the MEX68KDM Design Module. All pin numbers shown on the left side of Figure 1 are for MEX68KDM/EXORciser bus pin allocations. Other forms of buffering/termination may be used to suit the user's configuration. Gates U9, U11A, U10E, and U11B decode the address lines for address block \$18000 to \$1801F. The SSDA is located at \$18009 (mirrored at \$1800D) and \$1800B (mirrored at \$1800F).

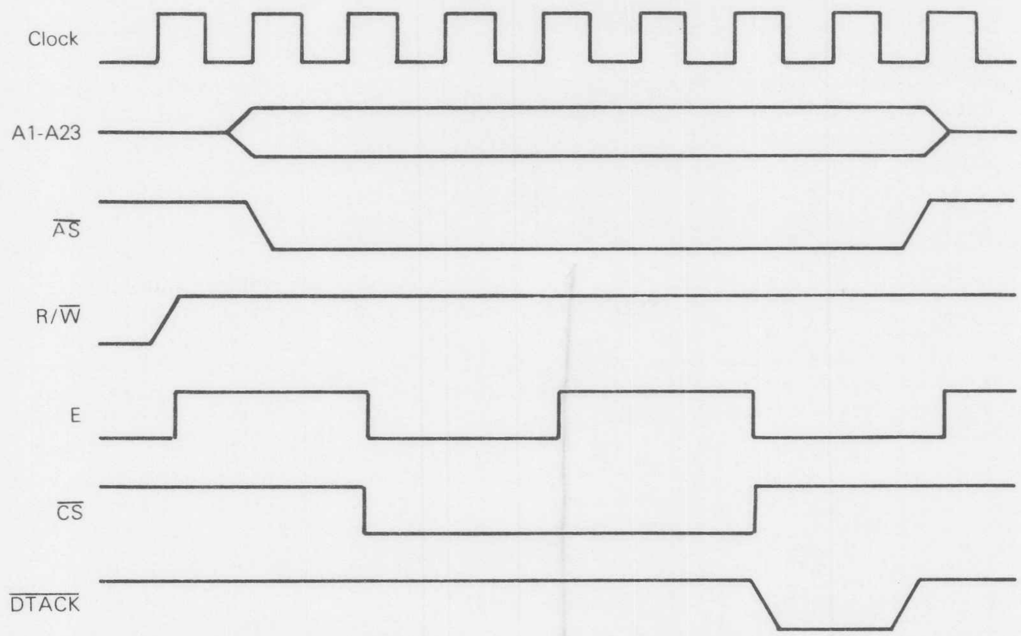
E Synchronization and RS Control — The continuous E signal which M6800 family peripherals require for operation will, in general, be asynchronous with MC68000 bus operation and, therefore, asynchronous with respect to chip select (pin 6, U11B). Flip-flop U13 serves to synchronize E with the chip select, supply chip select ($\overline{\text{CS}}$) to synchronize the peripheral part, and return $\overline{\text{DTACK}}$ to the asynchronous MC68000. Chip select (pin 6, U12B) is passed to the peripheral on the first falling edge of E past the assertion of CS (pin 6, U11B). This guarantees that there will always be sufficient setup time for the synchronous peripheral. Data transfer acknowledge (pin 8, U13B) is returned and $\overline{\text{CS}}$ removed from the peripheral on the next falling edge of E. Chip select for the peripheral is inverted by U10C and NANDed with address line A3 (pin 8, U12C) to complete the decoding and drive $\overline{\text{CS}}$ on the SSDA. Register select (RS) on the SSDA is driven by address line A1.



Device	Type
U1, U2, U3	MC8T97
U4	74LS09
U5, U6	74LS373
U9	74LS260
U10	74LS04
U11	74LS11
U12	74LS00
U13	74LS114
U16, U17	MC8T26
U20	74LS74
U21	MC68B52

Figure 1. MC68000/MC68B52 Interface — Schematic Diagram

READ CYCLE (Typical)



WRITE CYCLE (Typical)

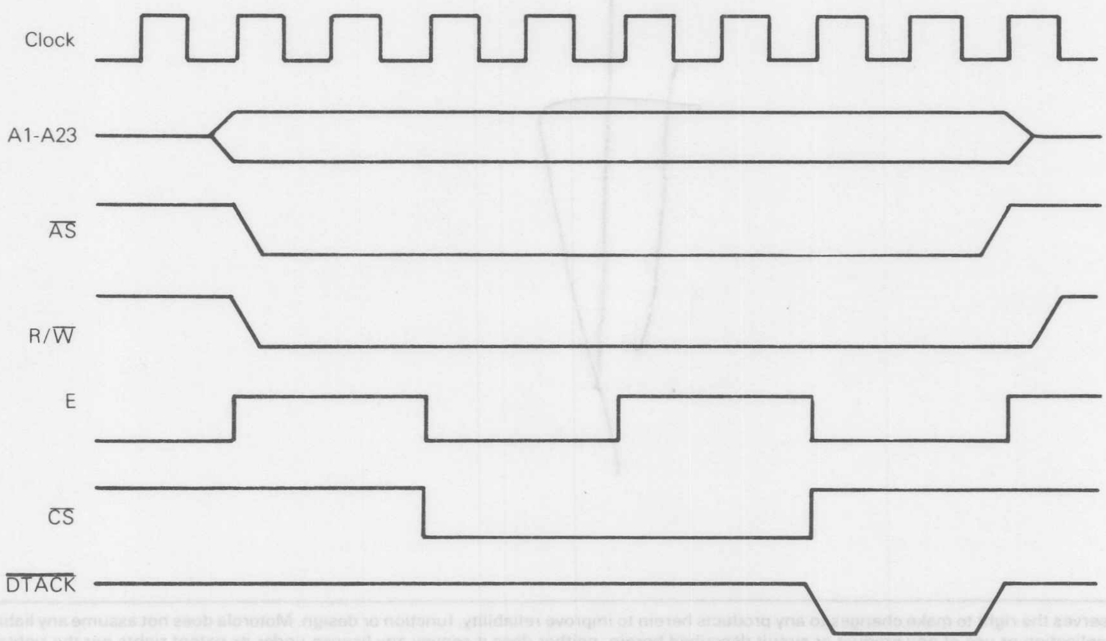


Figure 2. MC68000/MC68B52 Interface — Timing Diagrams

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Data Bus — The SSDA shown in Figure 1 is interfaced to the lower eight bits of the MC68000 data bus. Buffers U16 and U17 are inverting bidirectional buffers which make the interface compatible with the MEX68KDM Design Module. They may be omitted in any system which does not have an inverted data bus. In this case, U5 and U6 will provide sufficient bus buffering. Latches U5 and U6 are transparent 8-bit latches with three-state outputs which govern the flow of data to and from the SSDA. Gates U12A and U10D ensure that data is channeled toward the SSDA except when $\overline{\text{AS}}$ is low, CS is high, and R/$\overline{\text{W}}$ is high which prevents contention on the MC68000 bus itself. Data is latched on the rising edge of $\overline{\text{CS}}$ (pin 6, U12B) and held until the rising edge of $\overline{\text{DTACK}}$. This ensures that valid data is present on the MC68000 bus until the completion of a memory read cycle even though the synchronous peripheral may already be deselected. The transparency of the latches allows adequate data setup time on a memory cycle.

SYNCHRONOUS OPERATION

The SSDA may also be operated on the M6800 peripheral control bus provided by the MC68000. This bus consists of enable (E), valid memory address ($\overline{\text{VMA}}$), and valid peripheral address ($\overline{\text{VPA}}$). If the user wishes to use this feature of the MC68000, the circuitry of Figure 3 may be substituted for U13, U12B, and U4A of Figure 1. Valid peripheral address is returned to the MC68000 when chip select is detected. An open-collector gate is used because $\overline{\text{VPA}}$ is a wire ORed signal. When the processor repsonds with $\overline{\text{VMA}}$, the SSDA is selected. Enable (E) is derived from the system clock and provided directly by the MC68000. Therefore, if a clock frequency lower than eight megahertz is used, it may be desirable to replace U20A with an independent transmit/receive clock source to maintain high data transfer rates on the SSDA.

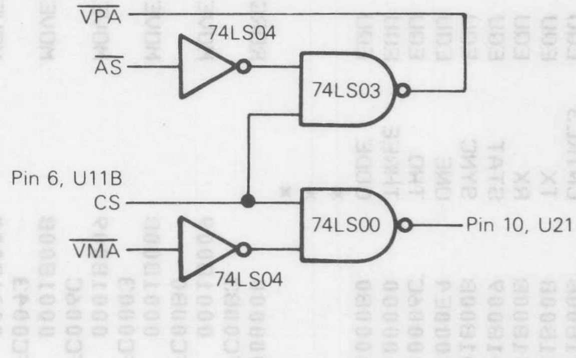
In general, this interface is slower than the asynchronous one.

PROGRAMMING THE SSDA

Figure 4 contains a typical initialization routine for the SSDA transmitter/receiver circuit shown in Figure 1. In this example, the SSDA is configured to transmit and receive 7-bit characters with odd parity. The transmitter is programmed to transmit sync code on underflow (transmitter FIFO empty) so as not to lose synchronization. The receiver is programmed to synchronize within two consecutive sync codes and to remove all sync characters ($80 in this case) that appear in the data stream. Interrupts from the receiver are enabled while transmitter availability and error detection must be checked by polling the status register.

CONCLUSION

The MC6852 is easily interfaced to the standard asynchronous bus of the MC68000 or the more conventional M6800 peripheral control bus. In either case, the MC6852 is a useful part in applications calling for synchronous protocol.



Note: When $\overline{\text{VMA}}$ is used, $\overline{\text{AS}}$ should be disconnected from the $\overline{\text{CS}}$ decoding (Figure 1, U11B) and that input tied active.

Figure 3. Synchronous Interface Circuitry

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REPORT52  MC68000 ASM REV= 1.0 - COPYRIGHT BY MOTOROLA 1978          PAGE

                              *
                              *                  EQUATES
                              *
            00000083          OPENS    EQU     $83            OPENS SYNC CODE WITH TX/RX RESET
            00000003          OPEN2    EQU     $03            OPENS CNTRL2 WITH TX/RX RESET
            00000043          OPEN3    EQU     $43            OPENS CNTRL3 WITH TX/RX RESET
            00018009          CNTRL1   EQU     $18009         LOCATION OF CONTROL REGISTER 1
            0001800B          CNTRL2   EQU     $1800B         LOCATION OF CONTROL REGISTER 2
            0001800B          CNTRL3   EQU     $1800B         LOCATION OF CONTROL REGISTER 3
            0001800B          TX       EQU     $1800B         LOCATION OF TRANSMITTER FIFO
            0001800B          RX       EQU     $1800B         LOCATION OF RECEIVER FIFO
            00018009          STAT     EQU     $18009         LOCATION OF STATUS REGISTER
            0001800B          SYNC     EQU     $1800B         LOCATION OF SYNC CODE REGISTER
            000000E4          ONE      EQU     $E4            INITIALIZATION OF CNTRL1
            0000006C          TWO      EQU     $6C            INITIALIZATION OF CNTRL2
            00000000          THREE    EQU     $00            INITIALIZATION OF CNTRL3
            00000080          CODE     EQU     $80            SYNCHRONIZATION CODE
                              *
                              *                  INITIALIZE THE SSDA
                              *
            00000000                   RORG    0
   000000 13FC0083
                0001B009               MOVE.B  #OPENS,CNTRL1  OPEN SYNC CODE
   000008 13FC0080
                0001B00B               MOVE.B  #CODE,SYNC     WRITE SYNC CODE
   000010 13FC0003
                0001B009               MOVE.B  #OPEN2,CNTRL1  OPEN CONTROL 2
   000018 13FC006C
                0001B00B               MOVE.B  #TWO,CNTRL2    TSU,7-BIT,ODD PARITY,1-BYTE,SM SET
   000020 13FC0043
                0001B009               MOVE.B  #OPEN3,CNTRL1  OPEN CONTROL 3
   000028 13FC0000
                0001B00B               MOVE.B  #THREE,CNTRL3  2-CHAR,INTERNAL SYNC
   000030 13FC00E4
                0001B009               MOVE.B  #ONE,CNTRL1    OPEN TX,RIE,STRIP SYNC
                              *
                              *
                              *
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Figure 4. Initialization Routine